Binary/Decimal Counter

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Laboratory exercise number:

Lab. 02

Second Partial

Laboratory exercise name:

Assignment 06

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| Names: | Roll Number | Date |
| Javier Mondragón M. | A01365137 | 4/October/2019 |

Lab description:

The purpose of this laboratory is to learn how program an FPGA using VHDL with the architecture “schematics” using the skills learnt in class. The purpose is to learn how to program in blocks using different components for future projects or complicated ones to be easier, faster to develop and easier to divide between a group.

The material used was:

Nexys 3 by Digilent for the FPGA

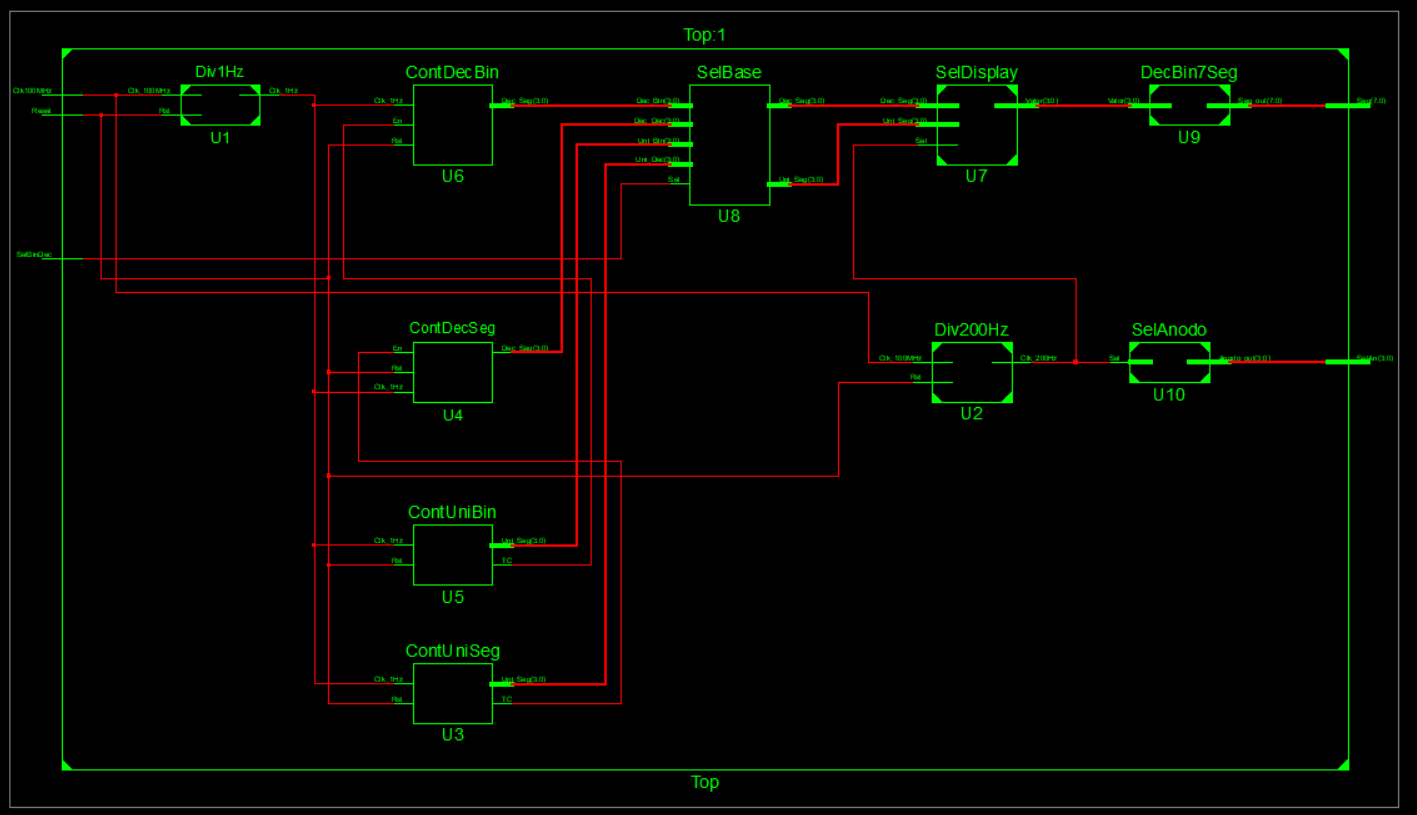
ISE Project Naviator for the VHDL compiler and editor

Adept by Digilent for the deployment to the FPGA

Schematics, block diagrams and/or timing diagrams:

The following project was developed with the diagram shown in image 1.1 and the code inside each block was developed in previous classes.

**Image 1.1**



*Diagram generated by the top diagram*

Results obtained:

The results obtained was successfully created a binary and decimal counter that is displayed in two different positions on the 7segment display which is in the Nexys.

**Image 2.1**

*Binary and Decimal counter working in FPGA*

**Image 2.2**

*Binary and Decimal counter working in FPGA*

**Image 2.3**

*Binary and Decimal counter working in FPGA*

Conclusions:

The use of a schematic and divide the program in blocks help to understand better and facilitate the develop. Also helps to find errors easier and make easier to distribute along a team a project.

Problems encountered:

The use of variables could complicate things when the unit and decimal counter were added. Is better if you evade them.